Inline Defect Part Average Testing (I-PAT™)

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April 25, 2018

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2018 Automotive Electronics Council Reliability Workshop

Outline

1. Introduction and Problem Statement
2. I-PAT Description
3. I-PAT Implementation Examples

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KLA-Tencor Overview

>40 years

Global Leader in Process Control since 1976

~23,000
tools installed worldwide

~6,400
global employees

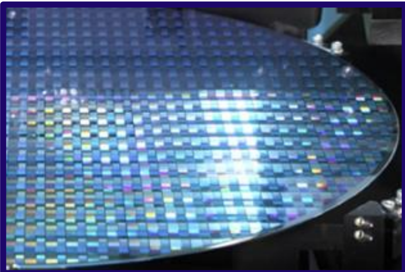
17
countries

$3.5B
FY17 revenue

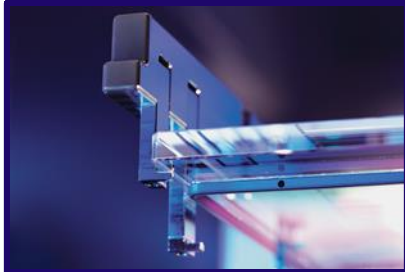
$2.1B
R&D investment over last 4 fiscal years

KLA-Tencor Markets Served

Semiconductor Manufacturing


IC Manufacturing

Wafer Manufacturing


Reticle Manufacturing

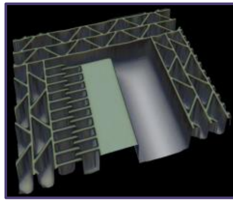
IC Packaging

Related Nanoelectronics Industries

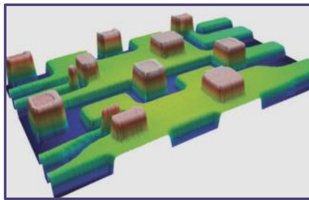
Compound Semiconductor

Power Device

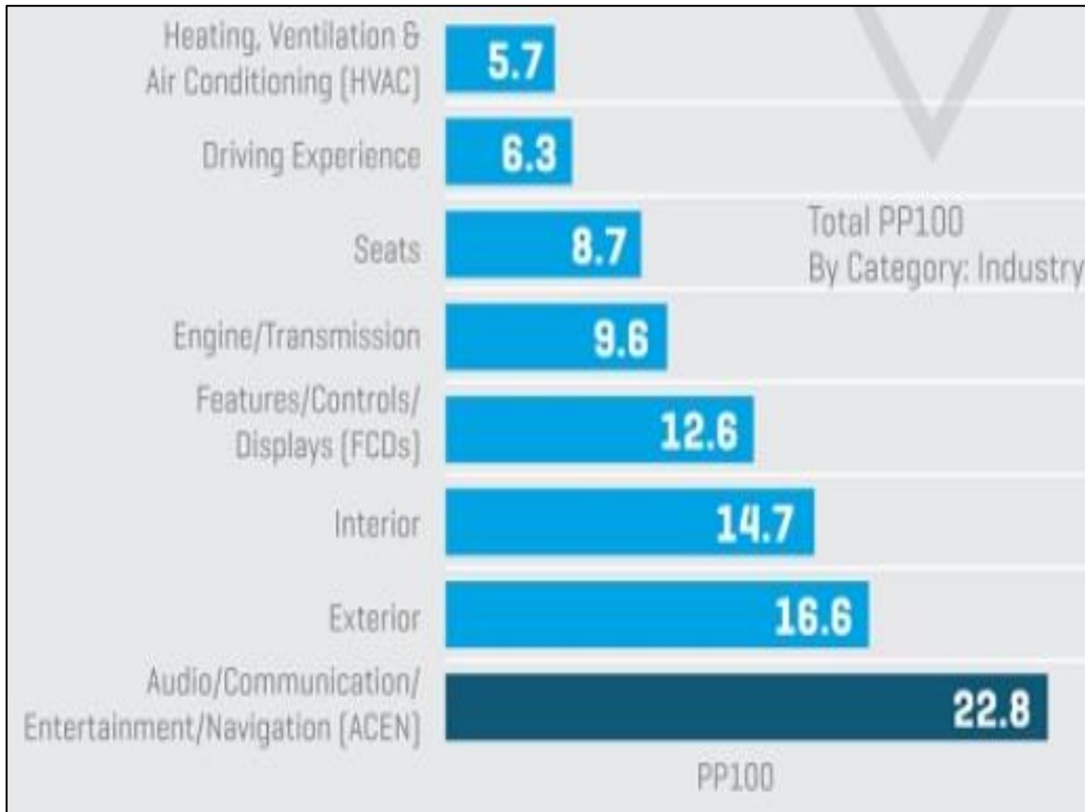
LED


MEMS

Data Storage / Media Head


General Purpose / Labs

Electronics is Already the #1 source of 0km Failures



- Shrinking Maturity Window
- Increasing Chip Content
- Increasing Quality Requirements
- Decreasing Test Coverage

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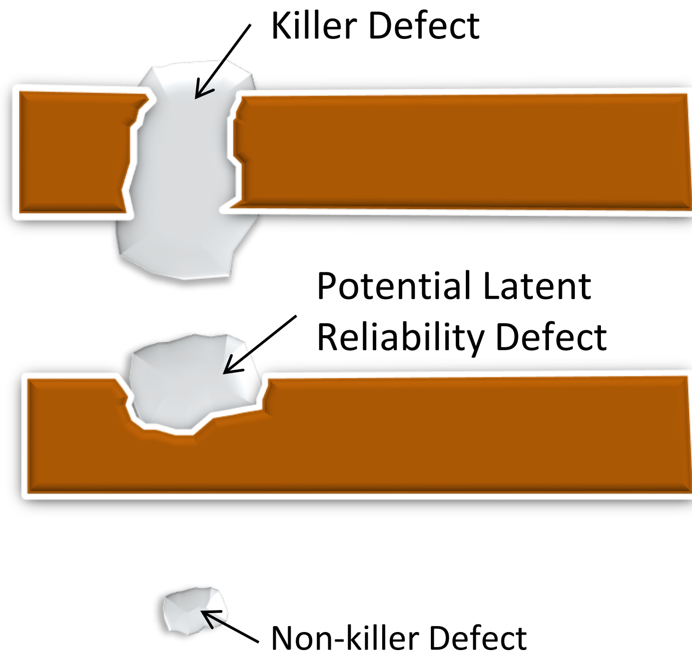
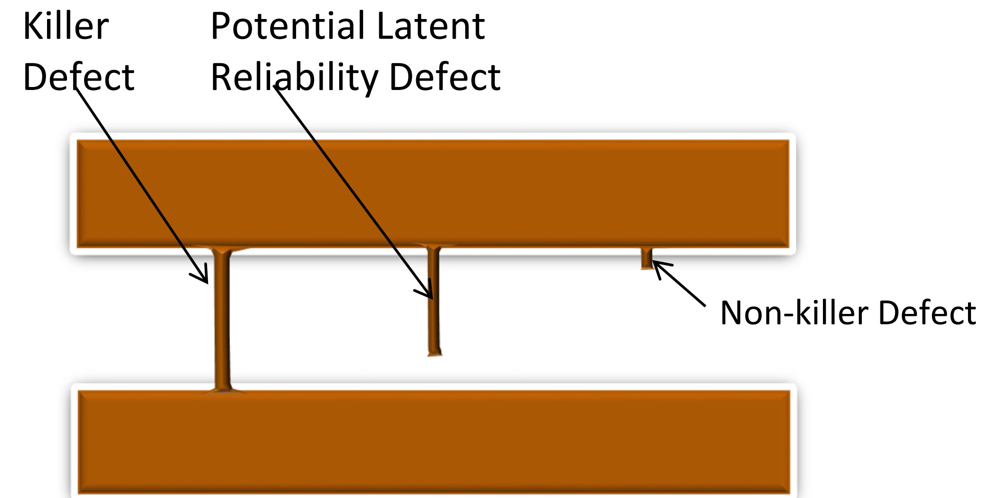
Latent Reliability Defects

1. The defect types that impact reliability are generally the same as those that impact yield. They are distinguished primarily by size and proximity to critical design features.





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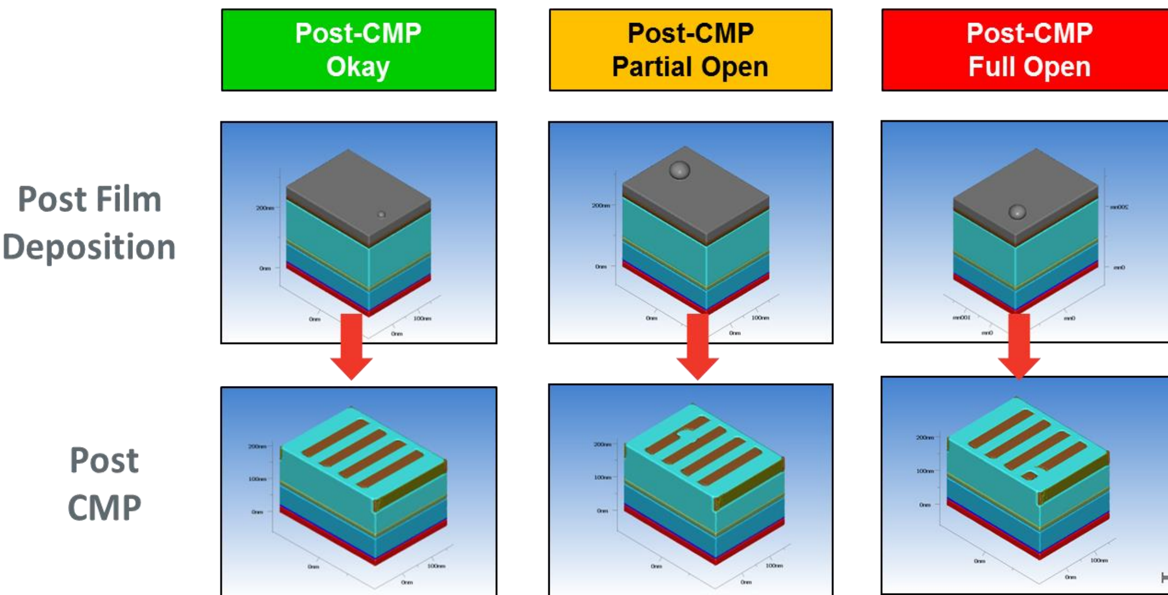
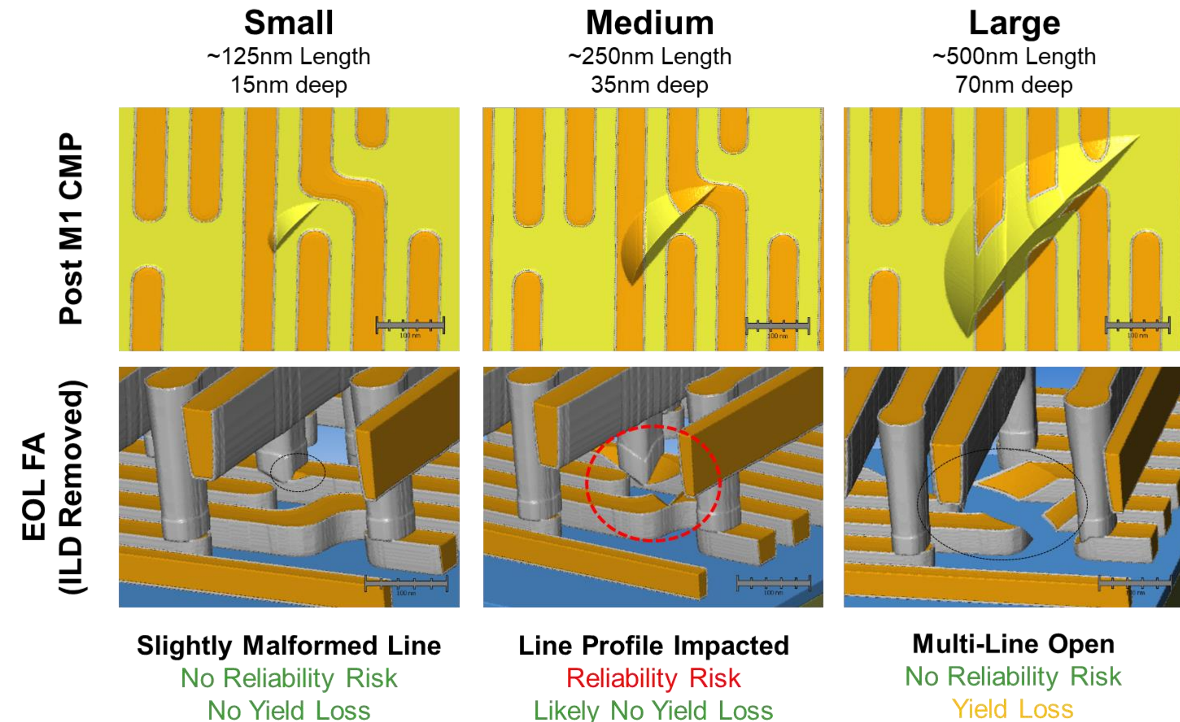
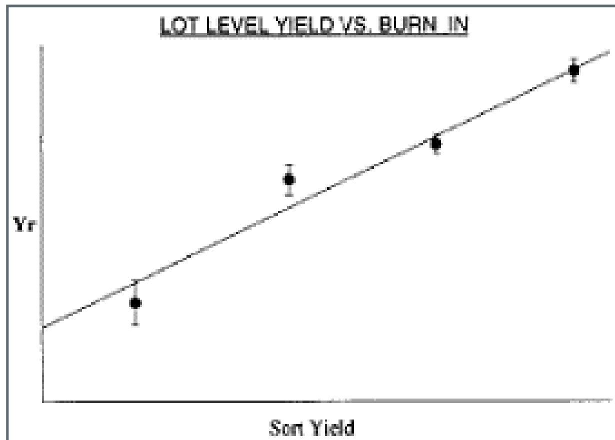


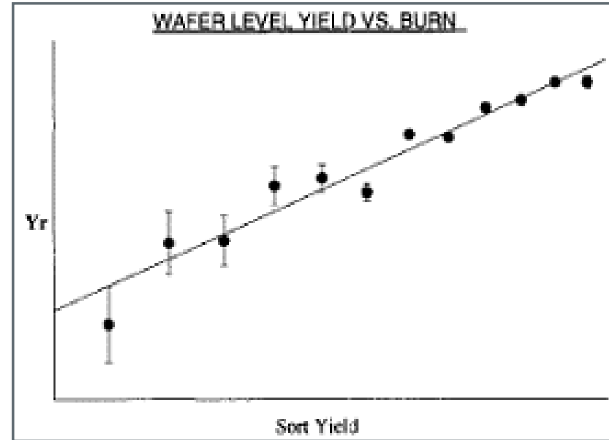


Latent Reliability Defects

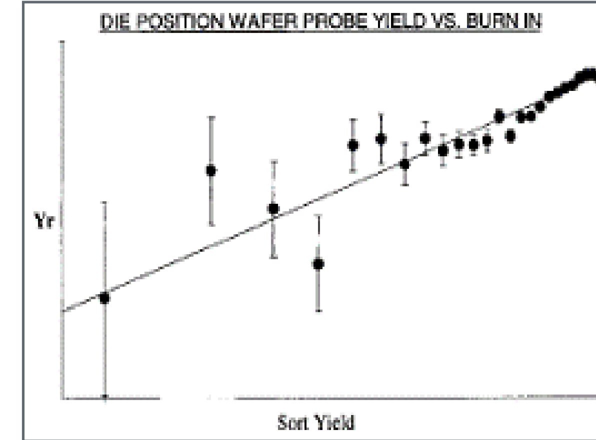
2. There is a direct correlation between yield and reliability at the lot, wafer, and die level. Total defectivity can be used as a proxy for LRD's.



Low yielding lots have degraded reliability



Low yielding wafers have degraded reliability

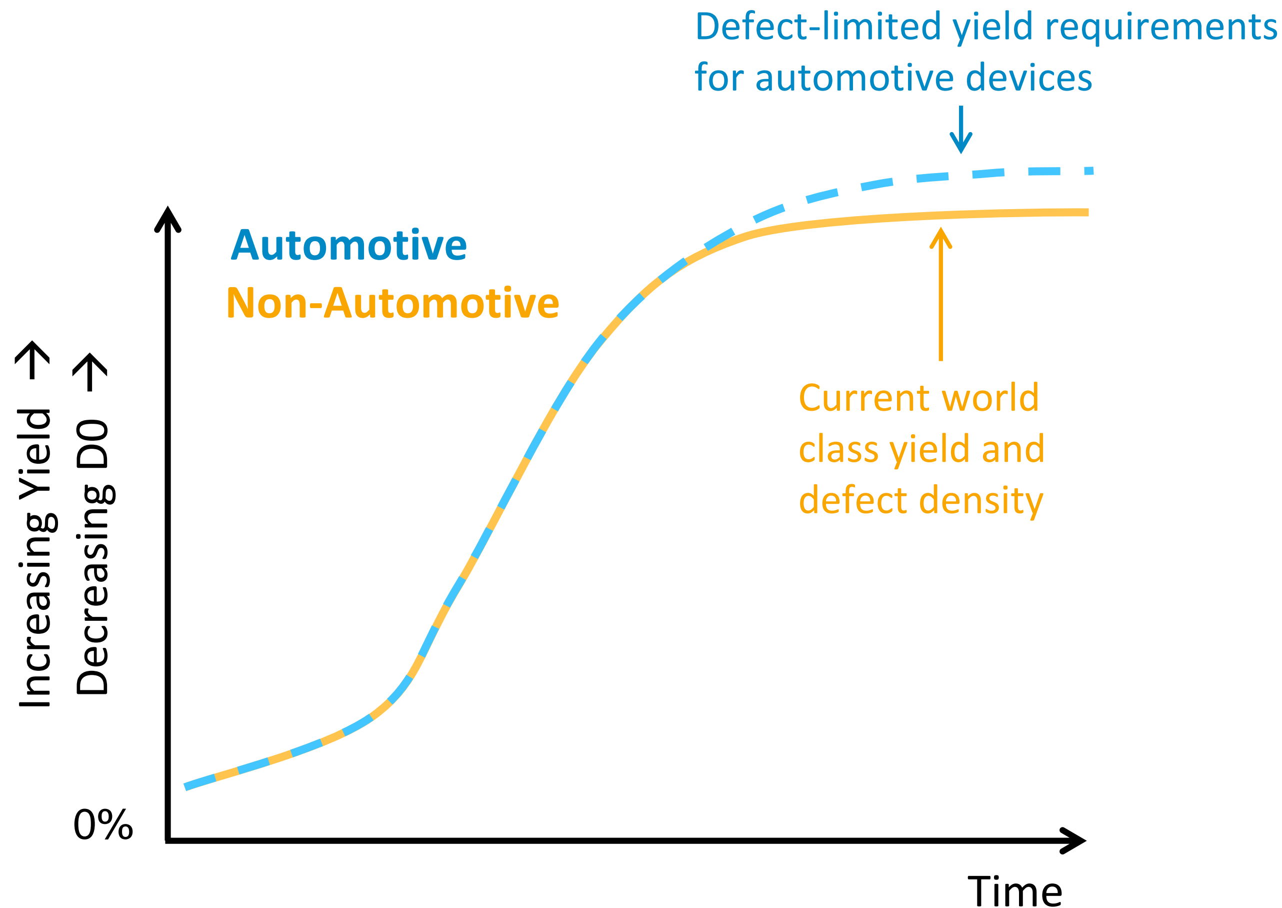


Low yielding die locations have degraded reliability

Riordan et al. (Intel) "Microprocessor Reliability Performance as a Function of Die Location for a .25um, Five Layer Metal CMOS Logic Process"

Latent Reliability Defects

3. The best way to reduce the possibility of latent reliability defect escapes is to reduce the fab's overall level of random defectivity.



1. Baseline Defect Reduction
2. Line Monitoring
3. **Die-Level Screening**

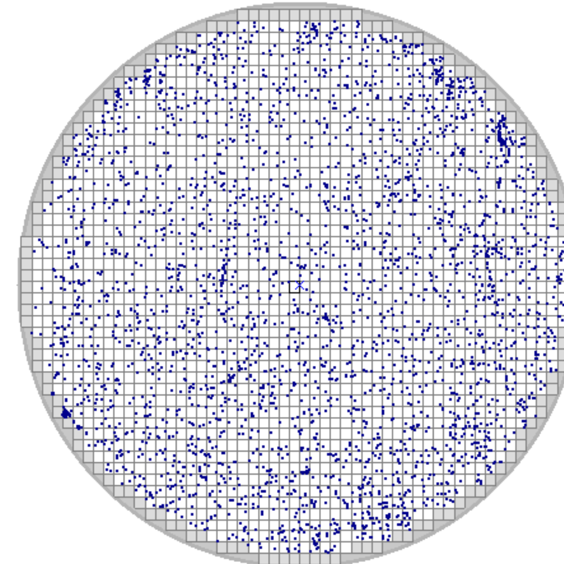
Die-Level Screening for Latent Reliability Defects?

Rationale:

- **On-wafer random defectivity** is one of the main culprits for 0km and field failures.
- Fabs already use of inline defect inspection for yield improvement and line monitoring.

Challenge:

- Only a very small fraction of defects produce latent reliability failures.



Need a statistical approach that can use machine learning to improve as we improve our understanding of latent defects.

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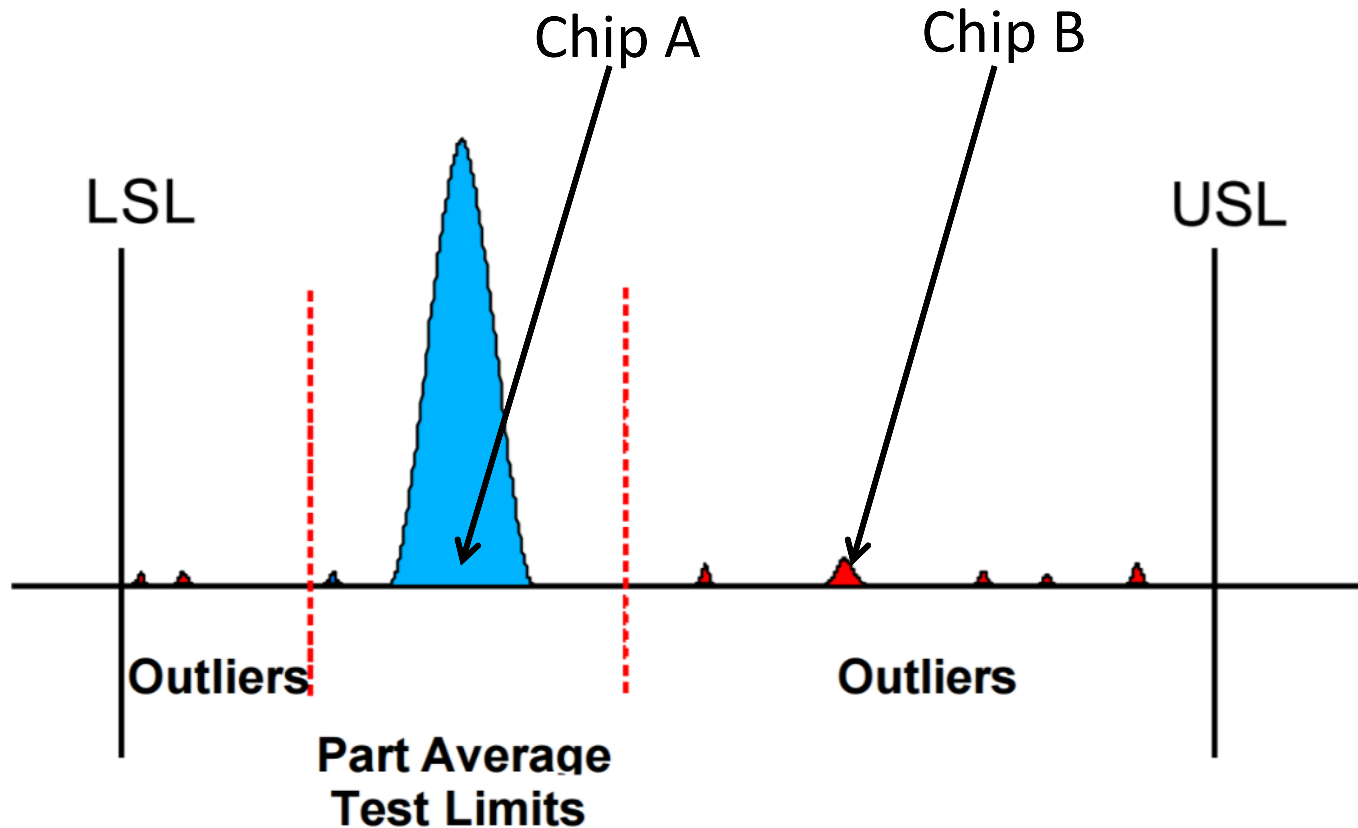
Part Average Testing

Is there a statistical difference in chip reliability between Chip A and B?



- Statistical screening technique
- Introduced by AEC in 1997

Inline Defect Part Average Testing (I-PAT)

Is there a statistical difference in chip reliability between Chip A and B?

- Inspection Layer 1 (LS)
- Inspection Layer 2 (LS)
- Inspection Layer 3 (macro)
- Inspection Layer 4 (LS)
- Inspection Layer 5 (BBP)
- Inspection Layer 6 (LS)
- Inspection Layer 7 (LS)
- Inspection Layer 8 (BBP)

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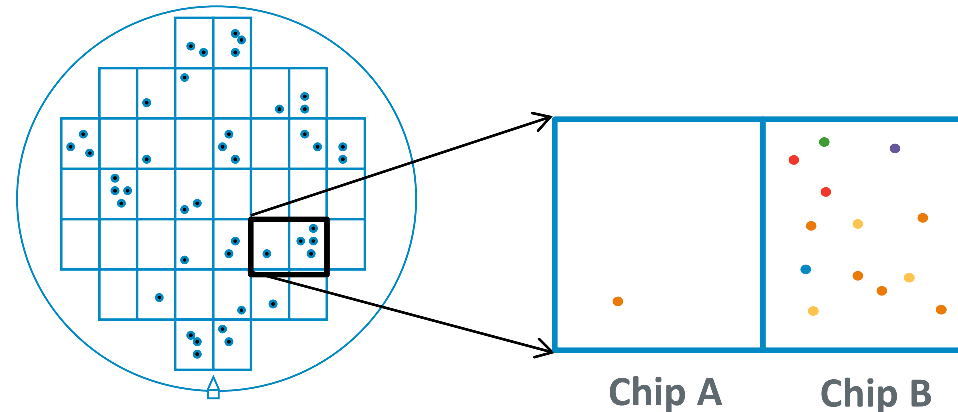
Inspection Layer N

Stacked-defect die map created by adding together the defects from multiple inline inspection steps



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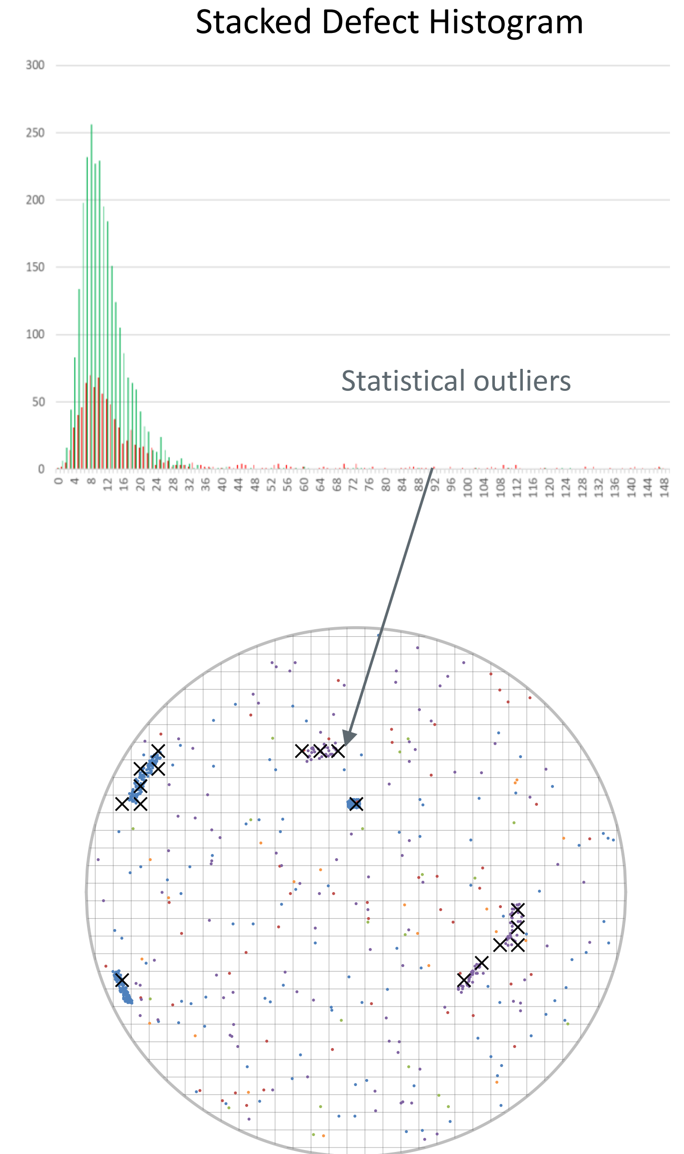
Inline Defect Part Average Testing (I-PAT)

I-PAT is the process of using inline defect data to selectively ink-off (i.e., map downgrade) die which have an elevated risk of latent reliability failures.

Key Elements

- Requires 100% inspection at key steps for the product(s) being screened. Results automatically → ink and scrap.
- Leverages the observed correlation between defectivity and reliability.
- Defect attributes, statistical filters, and advanced correlation engines are employed to improve capture and reduce overkill.



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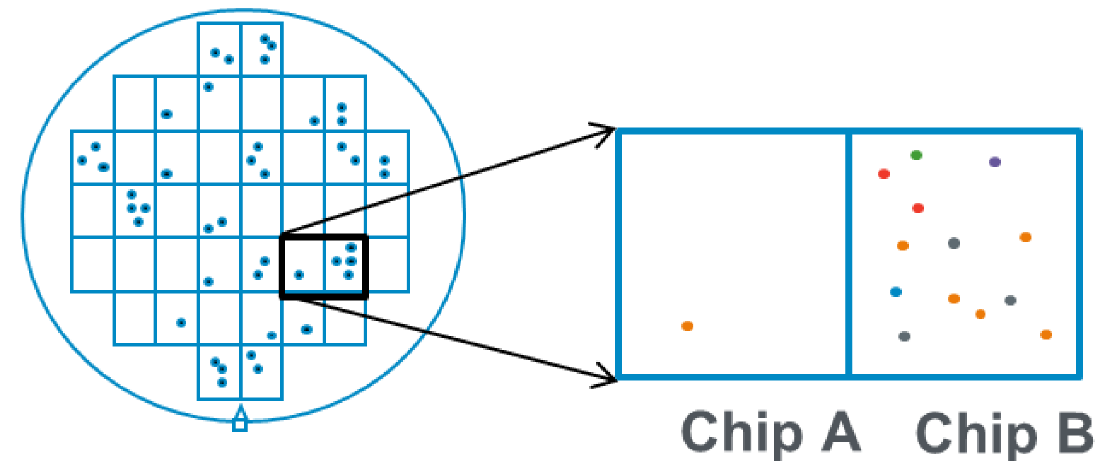
Simple I-PAT Implementation

Predicated on the observation that the probability distribution of latent defectivity roughly follows the distribution in total defectivity

$$P\,(LRD)_i \;=\; N_i\, m$$

The probability of die i having a latent reliability defect	=	The total number of defects in die i.	x	The ratio of latent reliability defects to total defectivity ($0 < m << 1$)



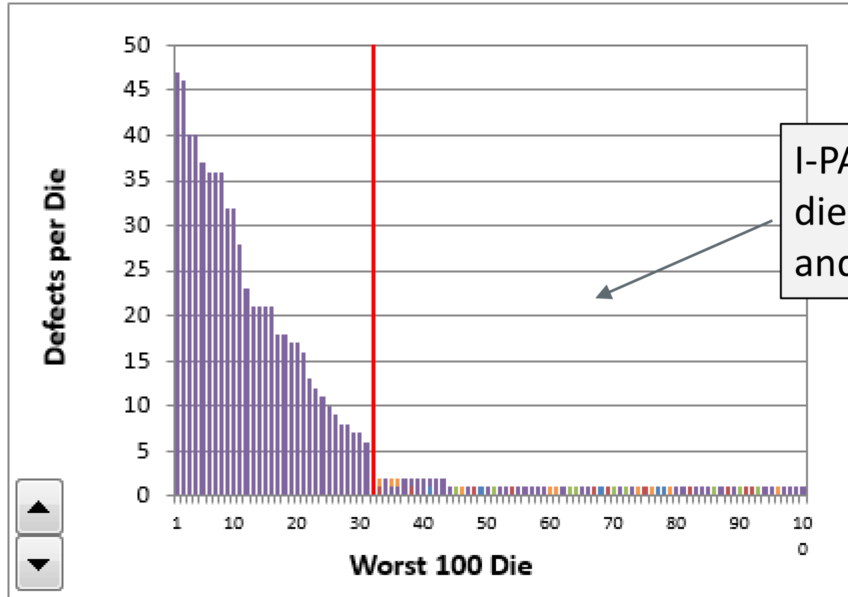
Chip B has a 15x higher statistical probability of a latent reliability failure than Chip A

Simple I-PAT

4 nominal layers
1 layers with small signature

Defects	AA	Gate	Contact	M1	M2
Profile	Flat	Flat	Flat	Scratches	Flat
Defects	25	25	25	800	25

Global	
Die Size (mm)	7.00
Die Area (mm^2)	49.00
Die / Waf (est)	1354
Failures	10

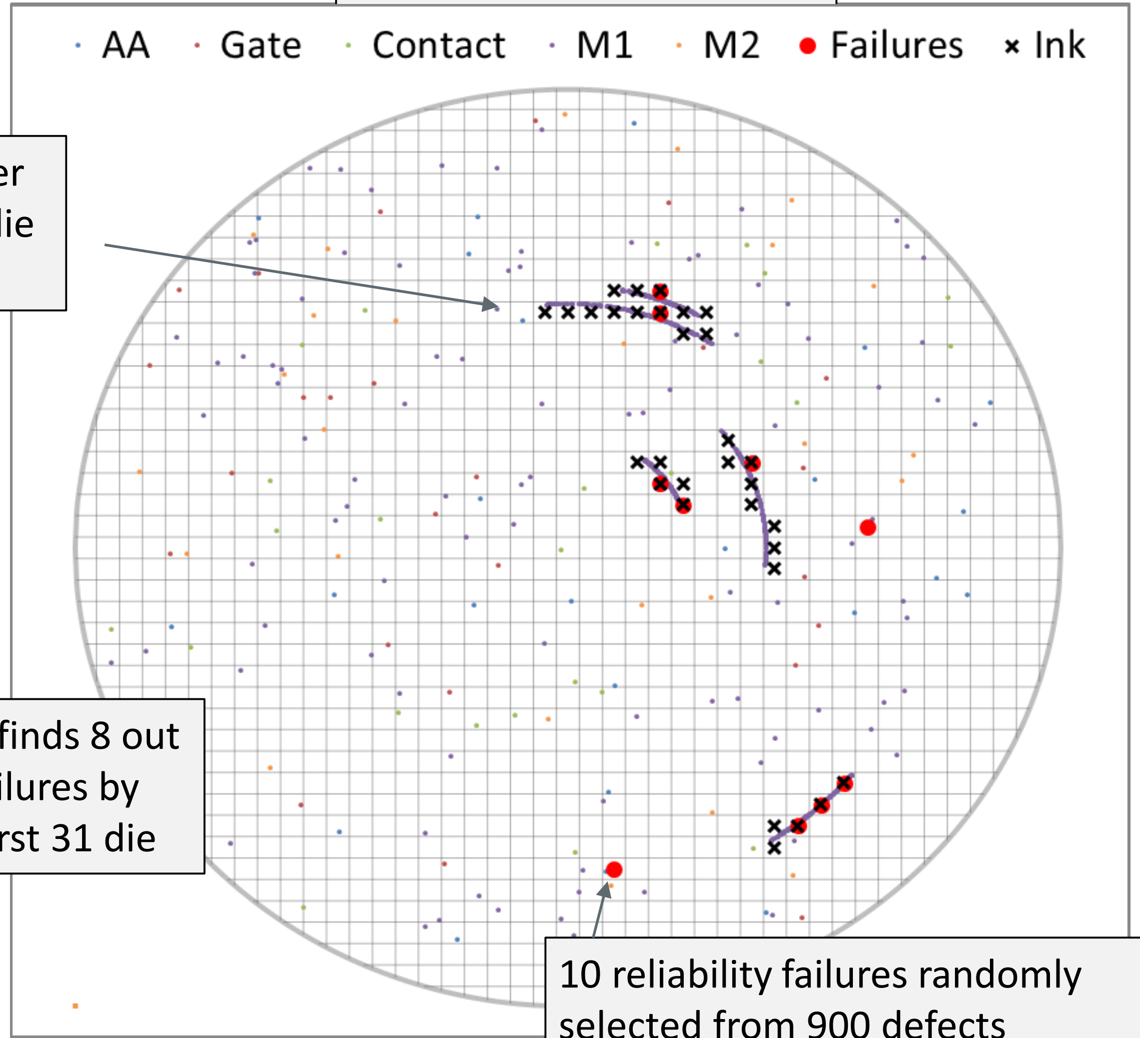


I-PAT identifies the outlier die based on # defects/die and inks them out (X).

Ink out die worse than # 32 (> 3)

	Failed	Inked	Inked %	Found	Found %
AA	1				
Gate	0				
Contact	0				
M1	9				
M2	0				
Stacked	10				
Total	**10**	**31**	**2.3%**	**8**	**80.0%**

Stacked defect wafer map



Simple I-PAT algo finds 8 out of 10 reliability failures by inking out the worst 31 die

10 reliability failures randomly selected from 900 defects

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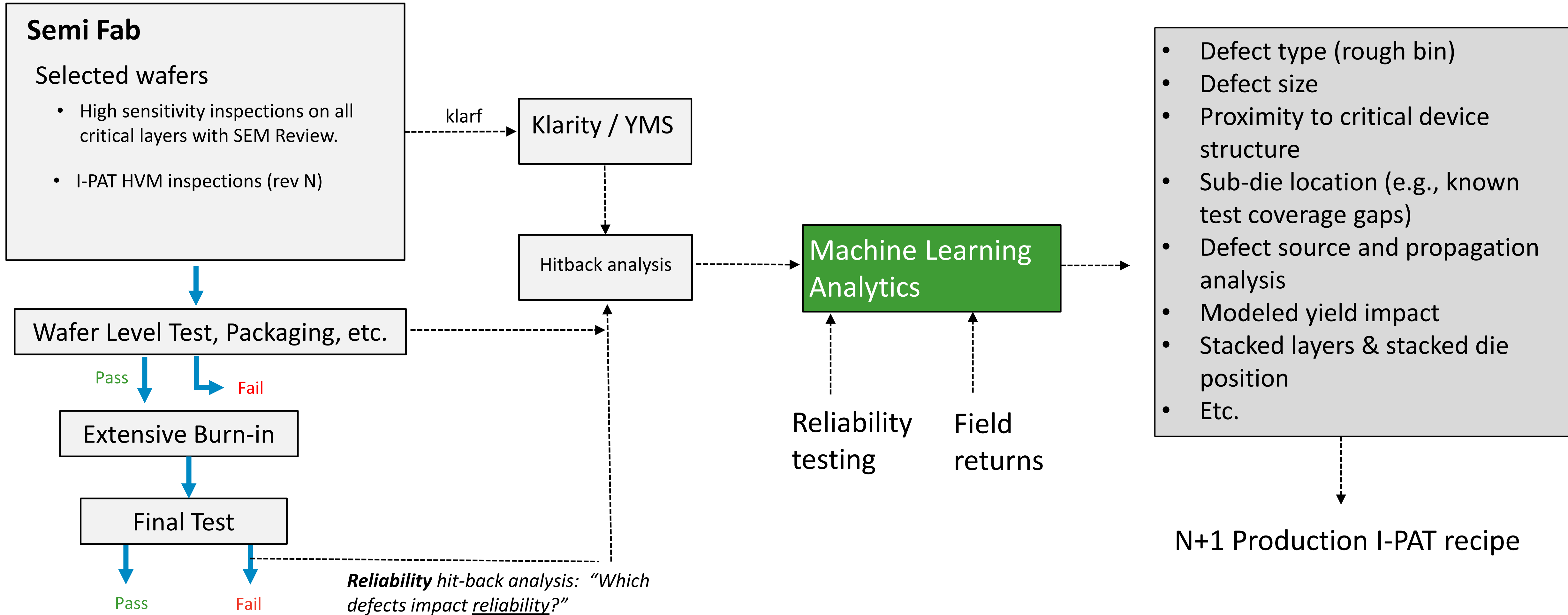
Smart I-PAT

Uses advanced correlation engines to weight defect probability based on defect attributes

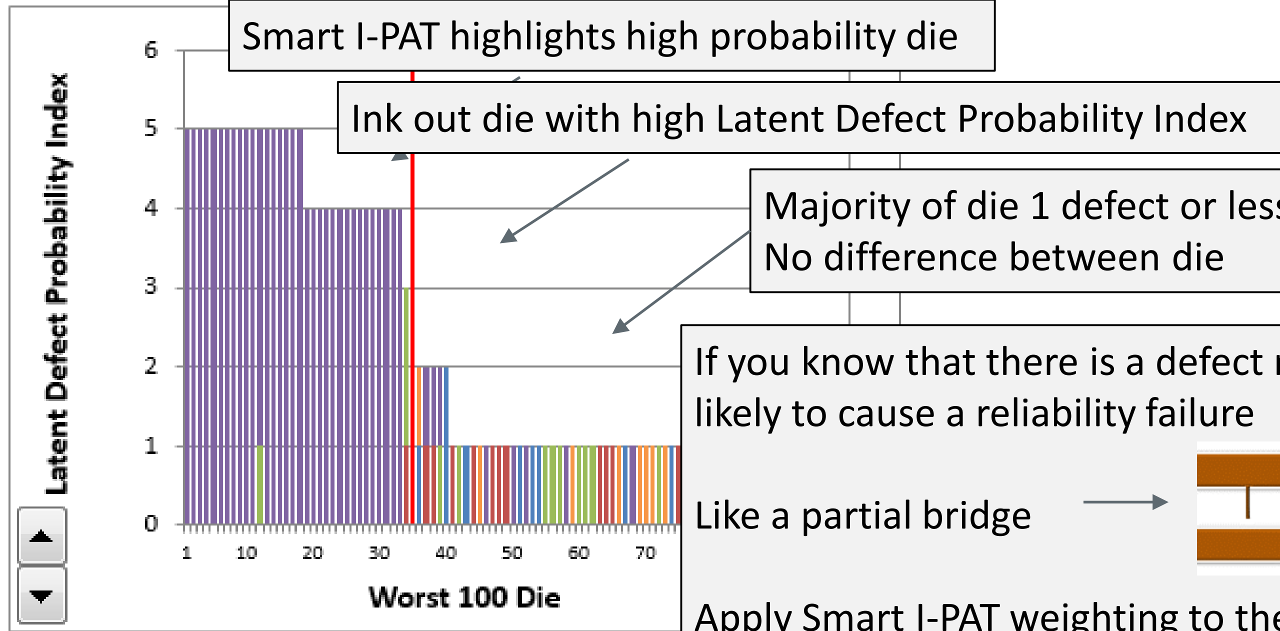


Smart I-PAT
Random Distribution

Completely random distribution in defectivity

Defects	AA	Gate	Contact	M1	M2
Profile	Flat	Flat	Flat	Flat	Flat
Defects	25	25	25	50	25

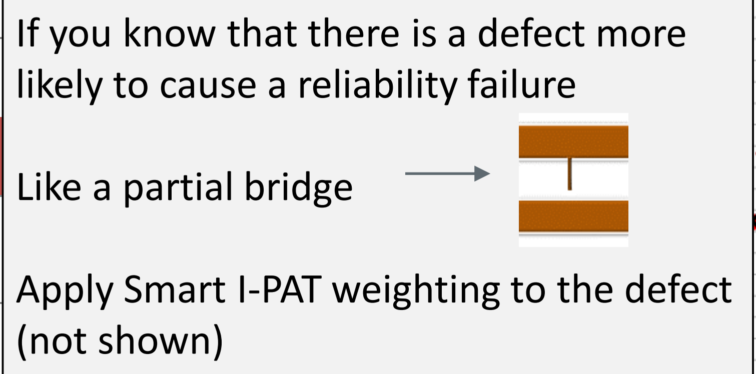
Global	
Die Size (mm)	7.00
Die Area (mm^2)	49.00
Die / Waf (est)	1354
Failures	10



Smart I-PAT highlights high probability die

Ink out die with high Latent Defect Probability Index

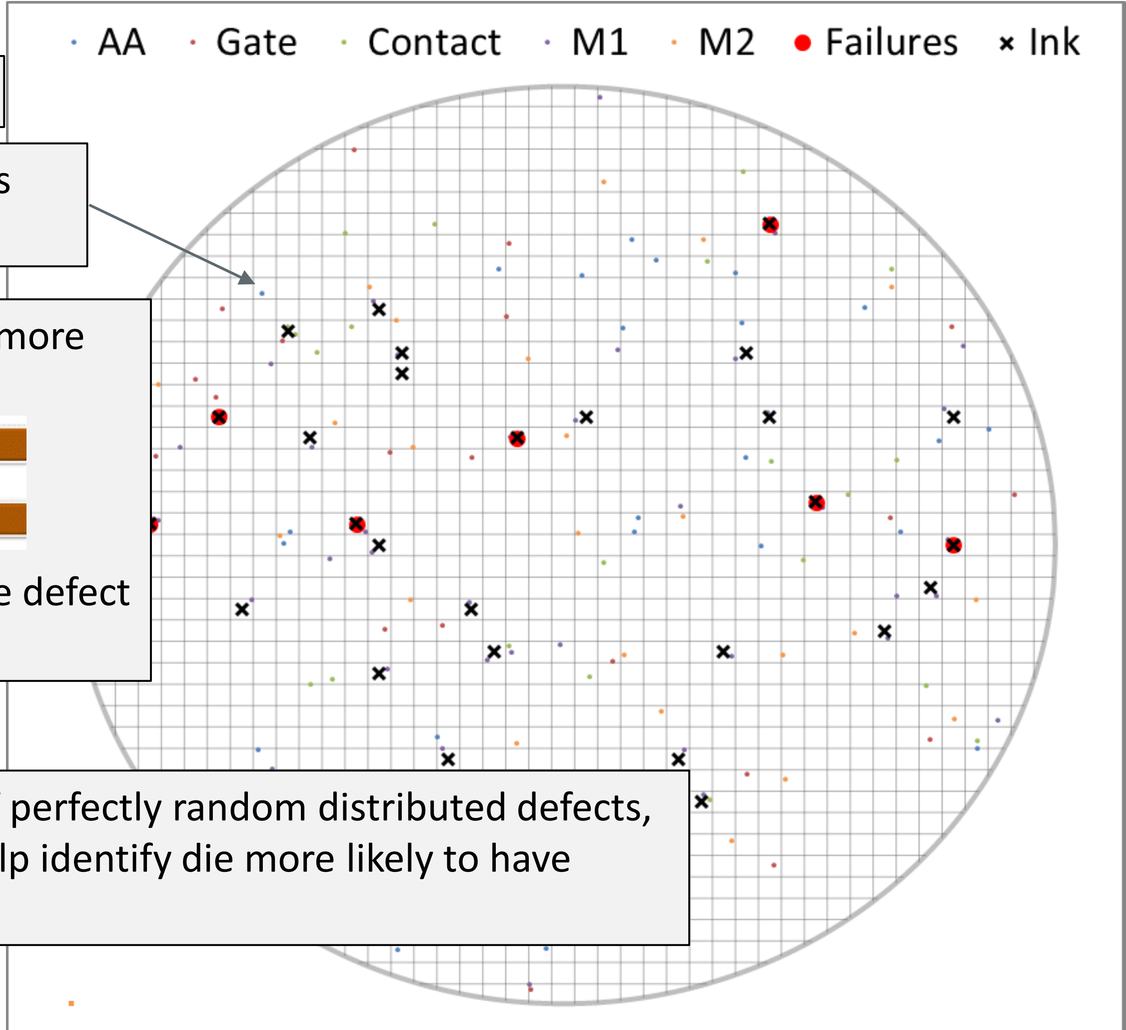
Majority of die 1 defect or less
No difference between die



If you know that there is a defect more likely to cause a reliability failure

Like a partial bridge

Apply Smart I-PAT weighting to the defect (not shown)



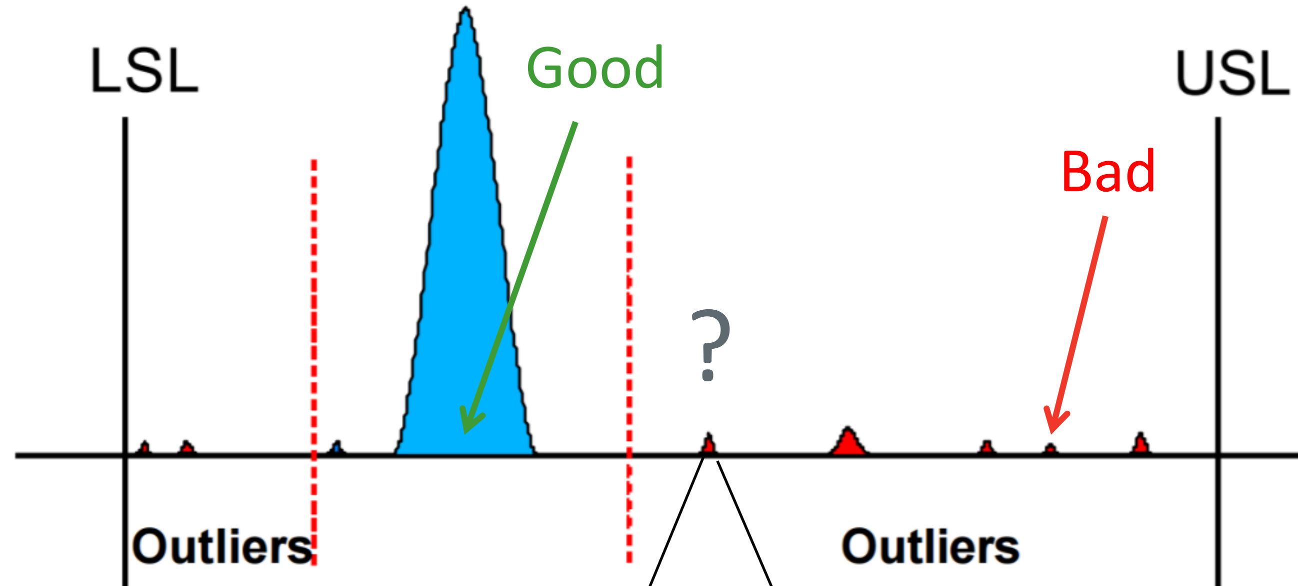
Ink out die worse than # 35 (> 2)

	Failed	Inked	Inked %	Found	Found %
AA	0				
Gate	0				
Contact	0				
M1	10				
M2	0				
Stacked	10				
Total	**10**	**34**	**2.5%**	**8**	**80.0%**

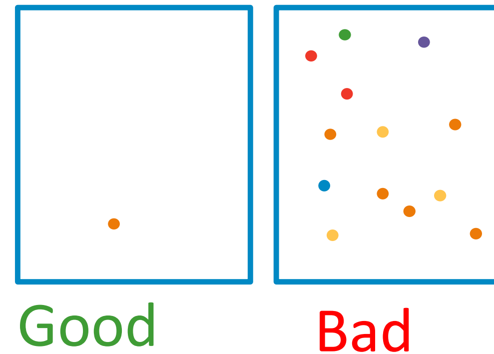
Even in the case of perfectly random distributed defects, Smart I-PAT can help identify die more likely to have reliability failures

Feed-Forward to Traditional P-PAT

P-PAT data



I-PAT

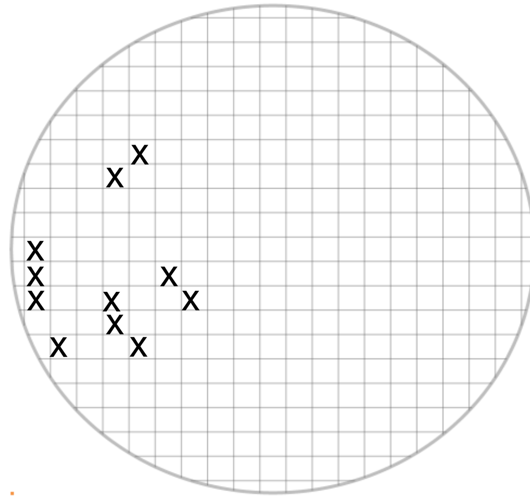


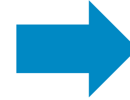
Good

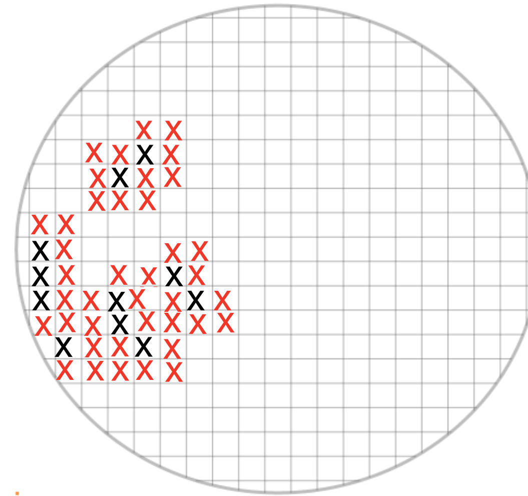
Bad

Feed-Forward to Traditional G-PAT

Bad Die at Probe

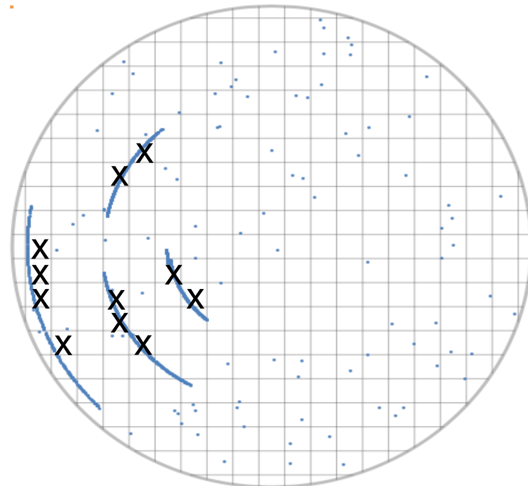


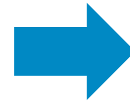


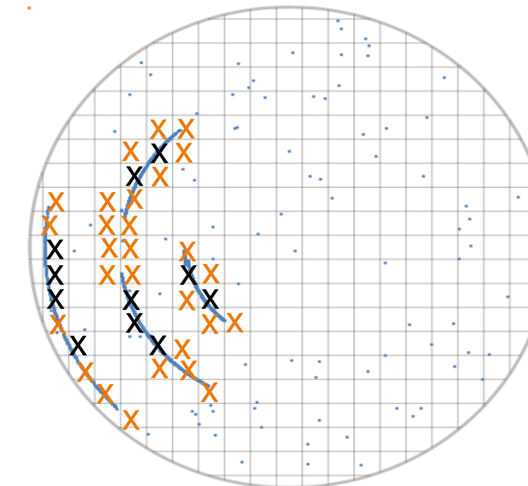


Standalone G-PAT (GDBN) inks off neighboring die

Bad Die at Probe with Defect Signature Overlay shows bad die are actually part of a larger signature







I-PAT + G-PAT together can more precisely ink off potential outlier die that are part of the underlying signature

Summary

1. The defect types that impact reliability are generally the same as those that impact yield. They are distinguished primarily by size and proximity to critical design features.

2. Reducing overall defectivity is the best way to reduce the potential for latent reliability defects. However, die-level screening is becoming necessary to meet the new standards for reliability.

3. Part Average Testing methodologies are now being applied to inline defect data (e.g., “I-PAT”) to improve capture of outlier die and reduce overkill from traditional PAT methods.

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